

**ABSTRACT OF THE DISCLOSURE**

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A2* → A system and technique provides fast acknowledgement and efficient servicing of interrupt sources coupled to a high latency path of an intermediate node of a computer network. The interrupt acknowledgement system avoids device accesses over the high latency path to thereby enable more efficient and faster acknowledgement of the interrupt sources. An external device coupled to the high latency path is provided with a separate interrupt signal for each type of interrupt supported by a processor of the intermediate node, such as an aggregation router. Each interrupt signal is directly fed to an interrupt multiplexing device over a first low latency path. The multiplexing device is accessible to the processor through a second low latency path. The external device asserts an interrupt by "pulsing" an appropriate interrupt signal to the multiplexing device. The multiplexing device maintains a current counter for each interrupt signal and increments that counter every time an interrupt pulse is detected. In addition to the counter, the multiplexing device maintains a status bit for each interrupt that is set whenever an interrupt is asserted and cleared whenever the bit is read.